THALES

1st national RISC-V student contest

Sponsored by Thales, the GDR SoC2 and the CNFM

FPGA optimisation of the ARIANE (CVA6) RISC-V core

You are students and like new challenges.
You are interested in computing architectures and want to participate in the design of the future European RISC-V embedded processors
Then join this contest and win up to € 5,000!

Context

Thales is a world leader for mission critical information systems for the security, defense, aerospace and ground transportation domains. It employs 80,000 people worldwide distributed in 68 countries. Today, Thales Research & Technology France, together with the GDR SoC2 and the CNFM, are proud to announce the co-organization of the 1st national RISC-V student contest in France on the FPGA optimisation of the ARIANE RISC-V core.

RISC-V is a recent open-source ISA that is gaining every day more attraction. From this ISA, ETH Zürich has designed a mid-range application core named **ARIANE**. It has the capacity to execute rich operating systems and integrates an MMU function and several privilege levels. More recently, an organization named **OpenHW Group** has been created with the ambition to design industrial-grade RISC-V processors. It has integrated the ARIANE core as its new application core under the name **CVA6**. INVIA, a Thales company, has created a more compact 32-bit version of the 64-bit original design, sharing the same source code.

ARIANE was primarily designed for ASIC targets, i.e. ICs that are synthesized over standard cells. Although the ARIANE source code can be compiled to FPGA matrices, e.g. for prototyping, further optimizations and smart architectural evolutions need to be brought to the design to increase its performance on FPGA targets. That is the focus of this student contest targeting French universities and engineering schools.

Targeted participants

You are a team of 1 to 4 students:

- 1 to 4 **Master 2 students** (or equivalent: final year in engineering schools)[1]
- 0 or 1 PhD student who started their curriculum after 2019-08-31
- Registered in a **French engineering school or university**
- Coached by a **supervising adviser** (usually a teacher, assistant professor, professor…)

You have the following skills or will get them:

- Digital electronics
- HDL languages
- Digital simulation
- Computing architecture
- Embedded programming

The timeline of the contest should make it a good fit for your last-year university/school project.

Description of the contest

Inputs

Thales will prepare a kit composed of:

- A testbench to simulate the **CVA6;**
- The parameters of the **CVA6** core to consider;
- A BSP;
- A reference design to run the **CVA6** core on an FPGA development board and the port of CoreMark.

The 32-bit version of the **CVA6** will be used. It will be obtained from the OpenHW Group or Thales GitHub repositories. The repository address will be communicated through the Piazza workspace (see below).

You will get support from the university/school and coaching from your adviser. The organizers (Thales, GdR SoC2, CNFM) will remain in contact with your adviser.

Communication and support

Supervising advisers (together with the university/school staff) will provide level 1 support to the team. Level 2 support may only be exercised if the issue cannot be solved at level 1.

A Piazza workspace will be created by the organizers to:

- Communicate announcements and practical information;
- Allow level 2 support;
- Host the student's forum;
- Host the organisers' and supervising advisers' forum.

The Piazza workspace will log messages so that teams, which will start later, can recover all past information. No mailing list will be maintained; all messages will go through the Piazza workspace after the team is registered. The address of the Piazza workspace will be communicated when the registration is accepted.

Prerequisites

Most parts of the CVA6 are written in **SystemVerilog**, a language widely adopted by the industry. You will have to use this language. Students who have followed a VHDL curriculum can follow the Mentor online course (30 days free[2]) to learn SystemVerilog fundamentals or other resources.

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[1] Although the contest does not primarily target M1 students, they are also accepted.

[2] Registration with your university email address.

The **FPGA development board** selected[3] for this context will be Digilent Zybo Z7-20. The list of necessary material is:

Reference	URL	List price	Remark
Zybo Z7-20	https://store.digilentinc.com/zybo-z7-zynq-7000-arm-fpga-soc-development-board/	$299.00	Zybo Z7-10 is too small for CVA6.
Pmod USBUART	https://store.digilentinc.com/pmod-usbuart-usb-to-uart-interface/	$9.99	Used for the console output
JTAG-HS2 Programming Cable	https://store.digilentinc.com/jtag-hs2-programming-cable/	$59.00	
Connectors	https://store.digilentinc.com/pmod-cable-kit-2x6-pin-and-2x6-pin-to-dual-6-pin-pmod-splitter-cable/	$5.99	At least a 6-pin connector Pmod is necessary; other references may offer it.

The complete set can be ordered by the supervising advisers from CNFM (contact: fpga@cnfm.fr).

A digital simulator will be needed. Thales will provide scripts for **Mentor Questa**. Other simulators can be used (without Thales support). Thales will support **Xilinx Vivado** for the synthesis.

CAD tools are available in schools/universities through CNFM. For any information, supervising advisers can contact cao@cnfm.fr.

Work to perform and constraints

You shall increase the **maximal frequency** and/or the **CoreMark** score of the CVA6 core on the FPGA matrix of the selected development board. The modifications shall not increase more than 50% the initial **core size** (LUT number).

You may perform local (e.g. reduce a critical path) or global optimizations (e.g. modify the pipeline, predictors…) in the core to increase the core performance.

Your creativity should prevail as long as:

- The **programming model** is not impacted, i.e. an existing binary running on the reference implementation shall still run on the optimized implementation.
- The following features are not removed (but may be optimized): MMU, floating-point operations, caches.

The resulting design shall still simulate correctly and execute correctly on the FPGA board, based on the kit provided by Thales.

Outputs

You shall provide:

- A report of maximum 30 pages
- A 20-slides PowerPoint presentation
- A link to your new source code uploaded on GitHub (under Apache 2.0 or Solderpad 2.0 licenses)
- The reports from the CAD tools that justify the results presented in the report.

A demonstrator with the FPGA board will be presented in front of a jury. It will highlight the performance increase.

Contributions to the OpenHW Group

Thales will promote some of the student open-source contributions to the OpenHW Group. The OpenHW Group criteria for accepting contributions may differ from those used in this contest.

[3] The Genesys 2 board listed in the pre-announcement was replaced by a cheaper board based on feedback.

Prizes and jury's criteria

To be eligible for the final selection, your solution must simulate correctly, work on the FPGA board and provide the correct results.

The jury will then rank the results based on:

1. Frequency increase (5 points /20)
2. CoreMark score increase per MHz (7 points /20)
3. Limited increase (or even better decrease) of FPGA resources (4 points /20)
4. Elegance of the solution (low impact on the original source code) (4 points /20)

For criteria 1 to 3, the points will be linearly distributed between the teams that get the lowest figure (no point) and the highest figure (all points). The points for criterion 4 will blend the number of modified lines and the jury's opinion.

Thales will award **€ 5,000** to the winning team and **€ 2,000** to the second best team (to be shared among the team).

Final selected teams will be given the opportunity to present their results at an event organized by Thales and/or the GdR SoC 2.

Registration

Teams may register anytime between **2020-09-25** and **2021-02-26** and run the contest at their own pace. They will recover past information through the Piazza workspace log.

Teams from a same university/school will register separately and can start at different dates.

Teams may deliver their results at any time before the end of the contest (**2020-04-23**). For instance, they can deliver their results in February if they start their internships in March.

To register, the supervising adviser will send an email to Jérôme Quévremont, Sébastien Pillement and Pascal Benoît (addresses below) with the following details:

- Name of the university/school
- Supervising adviser: Name, position (e.g. assistant professor), email address
- Name of the team (especially if there are several teams from a university/school)
- For each student: Name, option/major/"filière", email address
- Communication language: English or French (default).

The organizers will then check whether the registration is valid and send Piazza credentials to the students and the supervising adviser.

Alternatively, the supervising adviser can register alone and in a second step, register the students. This way, he/she can get the Piazza credentials early.

A few additional rules:

- Individual candidates and teams without a supervising adviser are not accepted.
- There may be several teams from a given university/school. A team may include students from different options/majors/"filières".
- If the university/school has a partnership with another university/school in France and Europe (e.g. ERASMUS program), some team members can be from these partner institutions.
- A student may not be in more than one team.
- An adviser may supervise several teams and ensure no co-operation between these teams on their technical solutions. Joint teaching/learning (e.g. SystemVerilog, ISA or architecture courses) is of course accepted and encouraged.
- The supervising adviser may be replaced during the project.
- Once the team is registered, the list of students shall not change (except under exceptional circumstances, with the organizers' agreement).

- The organizers will consider specific requests (if a situation is not clearly defined in the rules) while maintaining the fairness with other teams.

Abbreviations

ASIC	Application-Specific Integrated Circuit
BSP	Board Support Package
CAD	Computer-Aided Design
FPGA	Field-Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
ISA	Instruction Set Architecture
OS	Operating System
RISC	Reduction Instruction Set Computer
M1/M2	Master 1 / Master 2
MMU	Memory Management Unit
TBC	To be confirmed

Planning

	Thales	GdR SoC2	CNFM	Teams and universities/schools
September 25th, 2020	Launch the contest			Start registering teams (until 2020-02-26)
Until October 16th, 2020				The teams and their advisers can anticipate the contest: gaining knowledge on SystemVerilog, RISC-V and CVA6 (no support from the organizers)
October 18th, 2020	Deliver the kit for simulation and synthesis, provide guidelines			
December 7th, 2020	Deliver the kit for board-level development: reference design, BSP, CoreMark port.			
October-April	Level 2 support (fix bugs in the kits…)			Run the project. Advisers provide level 1 support to the student team.
April 23rd, 2021				**Deadline to submit results (reports, source code…)**
After April 23rd, 2021		Assess results		
	Ranking			
June 2021 (TBC)	Final event: prize announcement, presentation by the winning team			

Contacts

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